Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Canceled)

2. (Currently Amended) ~~The apparatus of claim 1~~ A transimpedance amplification apparatus with a signal source for generating a current signal, which comprises:

a source follower stage having a source follower structure, for receiving the current signal to reduce an impedance of the signal source;

a common source stage, following the source follower stage, driven by the reduced signal source impedance, for amplifying the current signal to extend a frequency bandwidth of the current signal and buffering the amplified signal with the extended frequency bandwidth thereof maintained, wherein the reduced signal source impedance serves to extend a frequency bandwidth of the common source stage; and

a shunt feedback resistor, which is installed between the source follower stage and the common source stage, for adjusting an input DC bias of the source follower stage and increasing a transimpedance gain of the common source stage, wherein the common source stage includes:

a first amplifying transistor for basically amplifying the current signal, wherein a gate thereof is connected to the source follower stage, while a drain thereof is coupled to a power supply and a source thereof is grounded;

a first buffering transistor for buffering the basically amplified signal with the bandwidth thereof maintained, wherein a gate thereof is connected to the drain of the first amplifying transistor, while a drain thereof is coupled to a power supply and a source is grounded;

a second amplifying transistor for secondarily amplifying the buffered signal, wherein a gate thereof is connected to the source of the first buffering transistor, while a drain thereof is coupled to a power supply and a source thereof is grounded; and

a second buffering transistor for adjusting the output impedance to be a predetermined value and buffering the secondarily amplified signal while maintaining frequency bandwidth thereof, wherein a gate thereof is connected to the drain of the second amplifying transistor, while a drain thereof is coupled to a power supply and a source thereof is grounded.

3. (Original) The apparatus of claim 2, wherein the shunt feedback resistor is installed between a gate of the source follower stage and the drain of the first amplifying transistor.

4. (Original) The apparatus of claim 3, wherein the predetermined value of the output impedance is about 50 Ohm.

5. (Currently Amended) The apparatus of claim 2, wherein the first amplifying transistor has an input frequency magnitude ω_{in} as follows:

$$\left[\left[\omega_{in} = \frac{1}{R_S[C_{GS} + (1 + g_m R_D) D_{GD}]}\right]\right] \underline{\omega_{in} = \frac{1}{R_S[C_{GS} + (1 + g_m R_D) C_{GD}]}} \quad \text{Eq. 1,}$$

wherein R_S is the signal source impedance; C_{GS} is a capacitance between the gate

and the source of the first amplifying transistor; C_{GD} is a capacitance between the gate and the drain of the first amplifying transistor; g_m is a transconductance of the first amplifying transistor; and R_D is a drain resistance of the first amplifying transistor.

6. (Original) The apparatus of claim 5, wherein the source follower stage has an output impedance as follows:

$$Z_{out} = \frac{sR_S'C_{GS}'+1}{g_m'+sC_{GS}'},$$

wherein C_{GS}' is a capacitance between the gate and the source of the source follower stage; g_m' is a transconductance of the source follower stage; and "s" is a complex frequency parameter.

7. (Original) The apparatus of claim 6, wherein each transistor is a FET (Field Effect Transistor) device.

8. (Original) The apparatus of claim 6, wherein each transistor is a BJT (Bipolar Junction Transistor) device.